FIG. 1

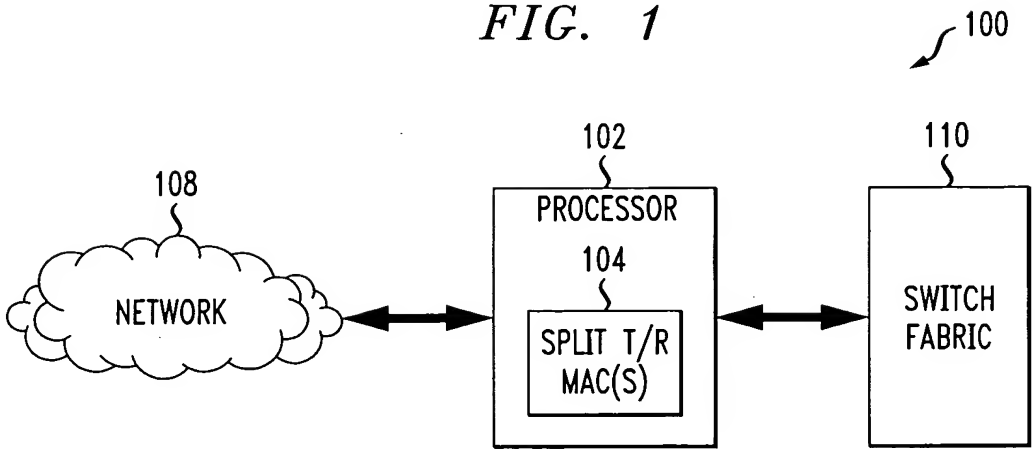


FIG. 2

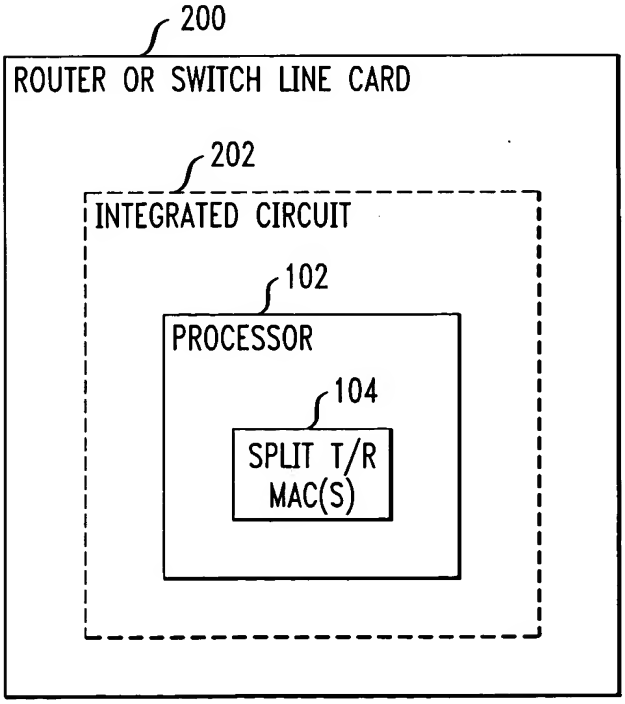
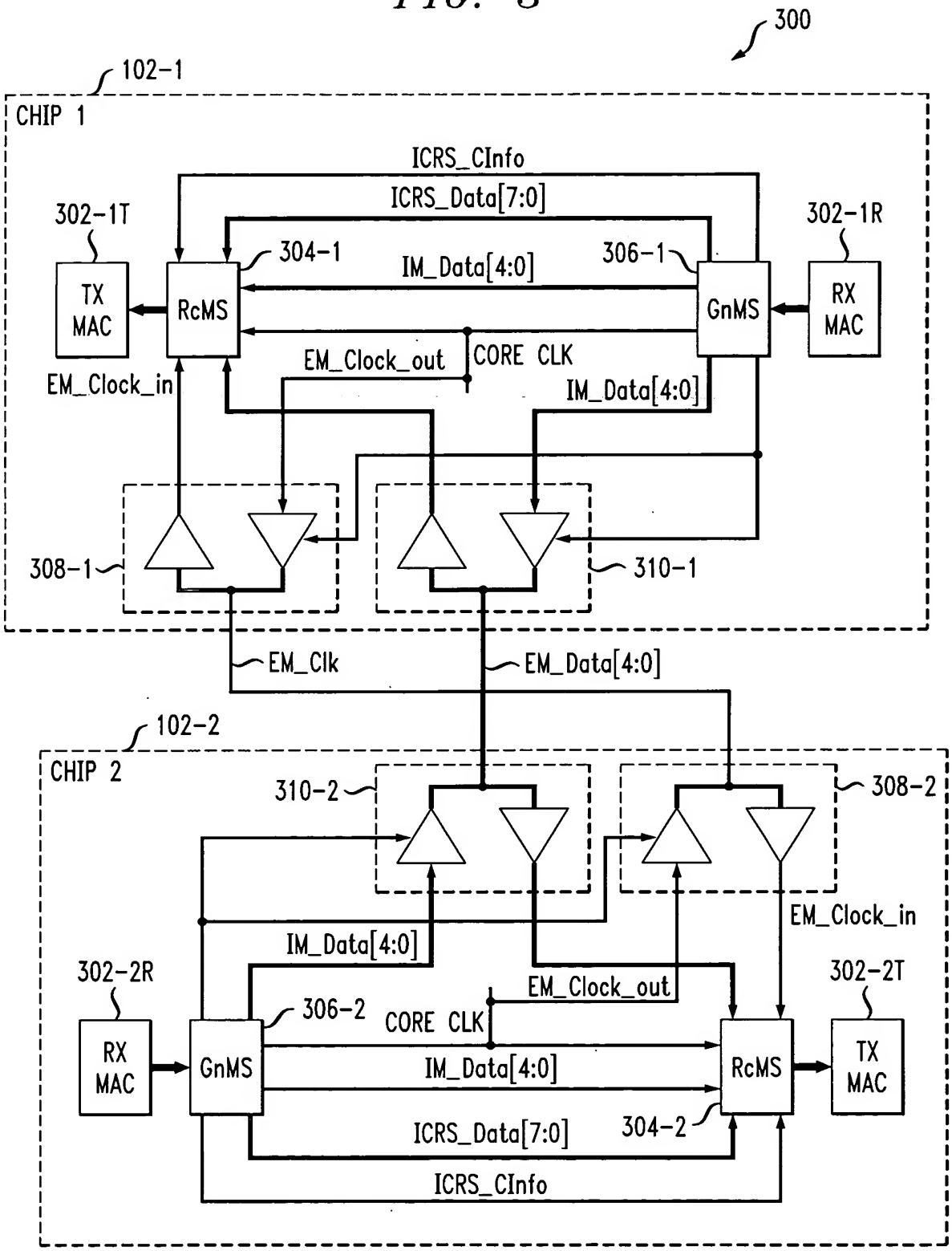


FIG. 3



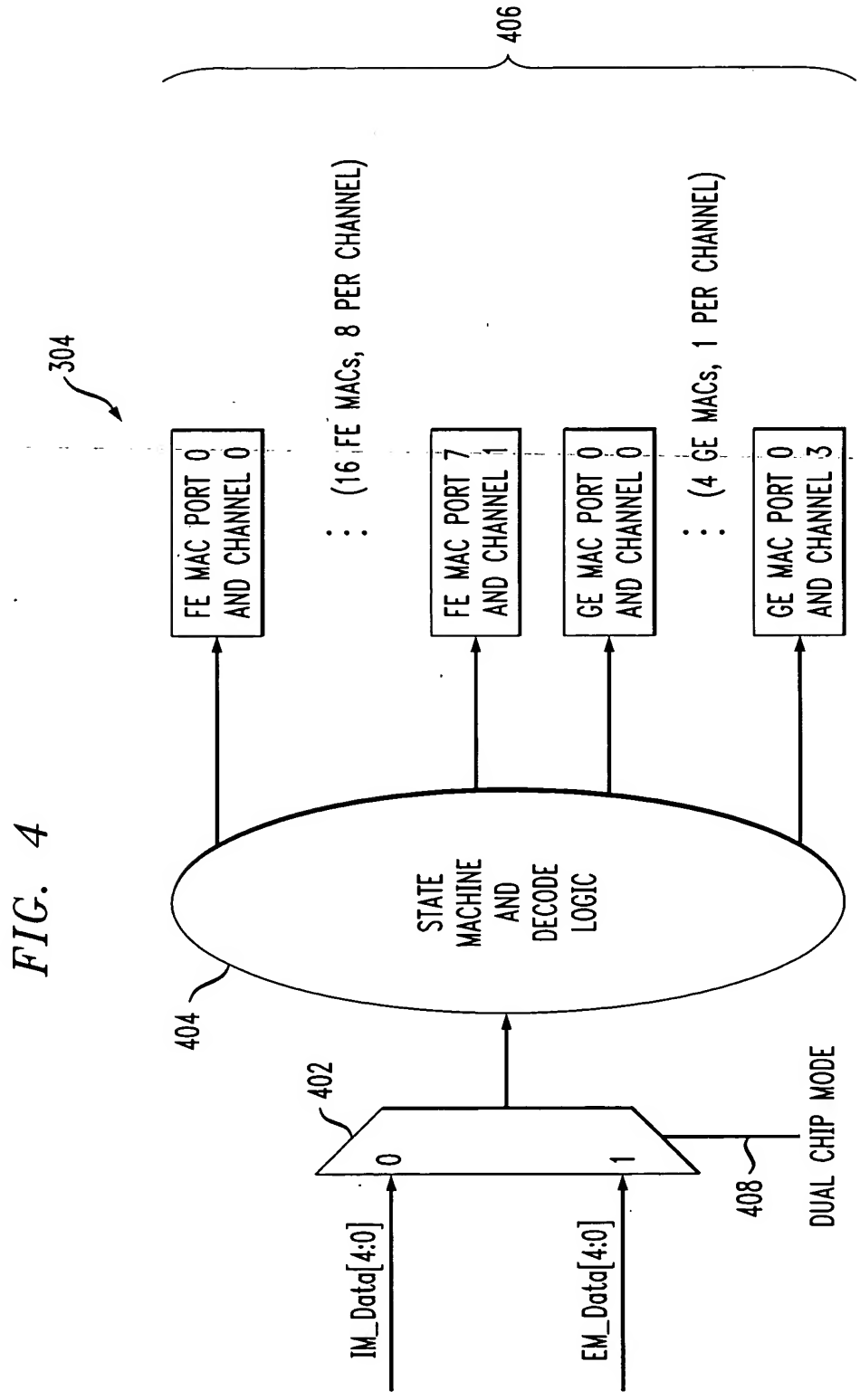


FIG. 4

FIG. 5

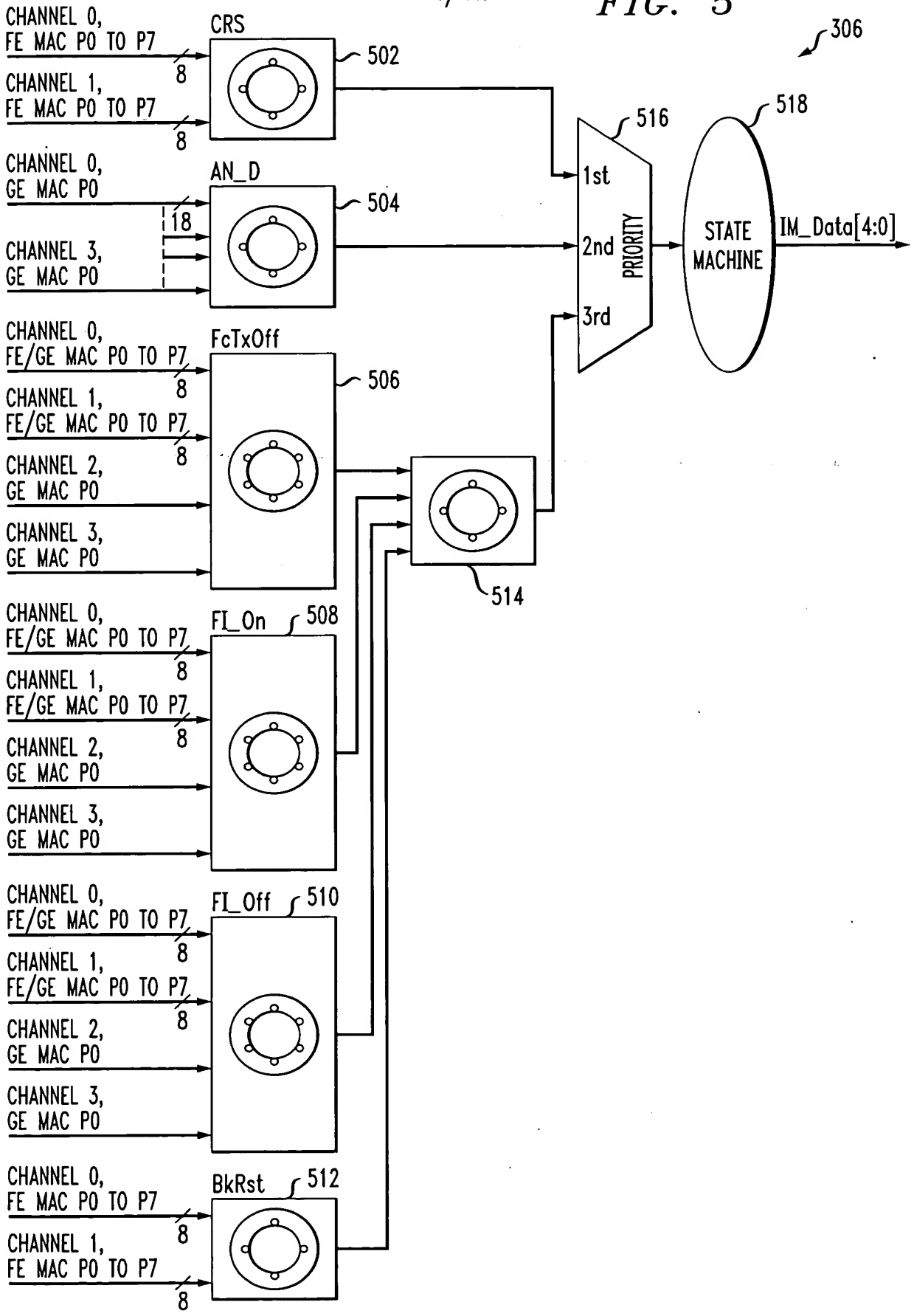


FIG. 6

ADDR DECODING FOR CRS FOR FE MAC RX

CHANNEL ADDR[1:0]	NIBBLE ADDR	[3:0]	BIT 0	BIT 1	BIT 2	BIT 3
00	0	CRS_C00_s	CRS_C0P0_s	CRS_C0P1_s	CRS_C0P2_s	CRS_C0P3_s
00	1	CRS_C01_s	CRS_C0P4_s	CRS_C0P5_s	CRS_C0P6_s	CRS_C0P7_s
01	0	CRS_C10_s	CRS_C1P0_s	CRS_C1P1_s	CRS_C1P2_s	CRS_C1P3_s
01	1	CRS_C11_s	CRS_C1P4_s	CRS_C1P5_s	CRS_C1P6_s	CRS_C1P7_s
10	0	CRS_C20_s	CRS_C2P0_s	CRS_C2P1_s	CRS_C2P2_s	CRS_C2P3_s
10	1	CRS_C21_s	CRS_C2P4_s	CRS_C2P5_s	CRS_C2P6_s	CRS_C2P7_s
11	0	CRS_C30_s	CRS_C3P0_s	CRS_C3P1_s	CRS_C3P2_s	CRS_C3P3_s
11	1	CRS_C31_s	CRS_C3P4_s	CRS_C3P5_s	CRS_C3P6_s	CRS_C3P7_s

FIG. 7

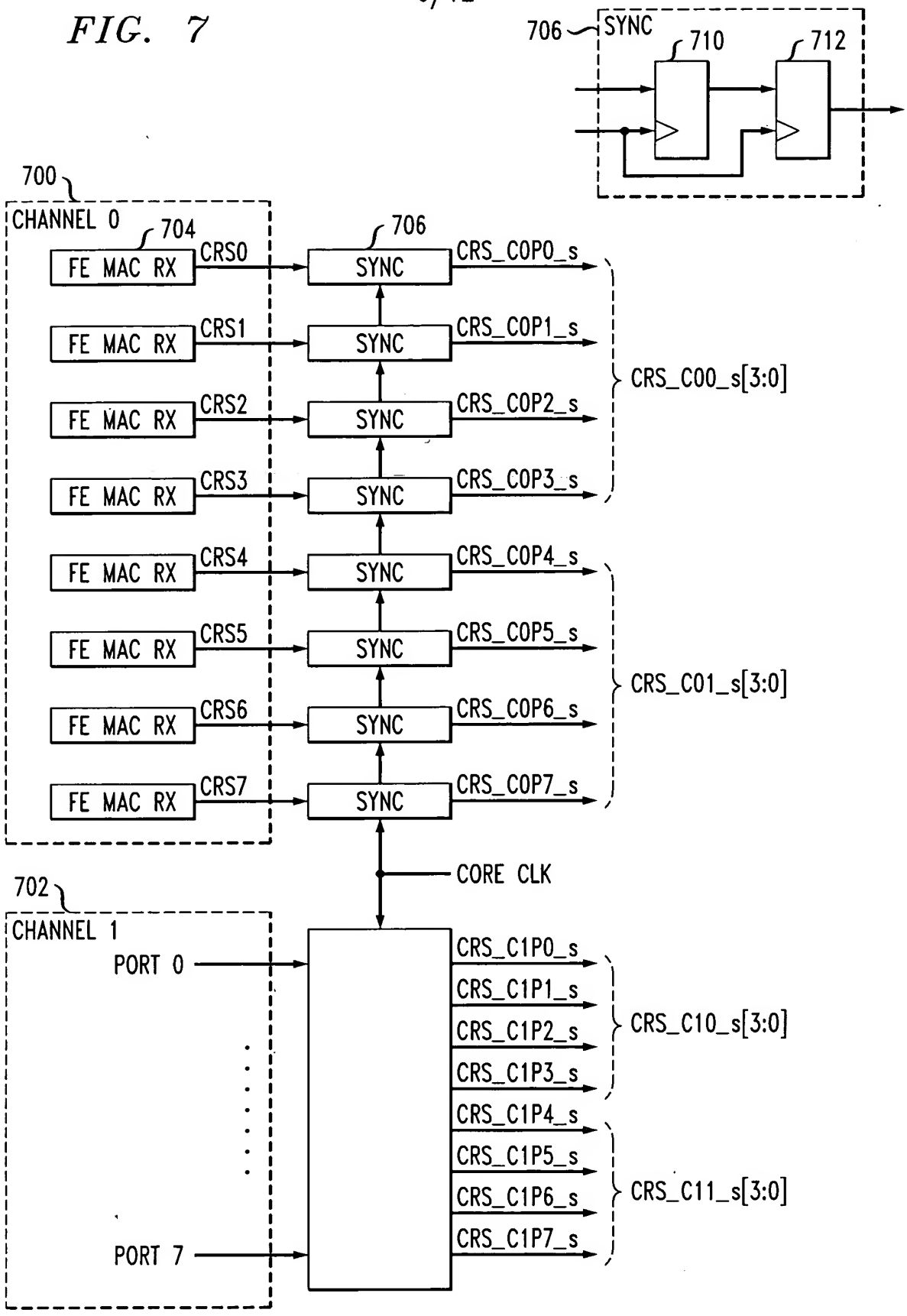


FIG. 8

ADDR DECODING FOR BkRst FOR 16 FE MAC RX

CHANNEL ADDR[1:0]	NIBBLE ADDR	[3:0]	BIT 0	BIT 1	BIT 2	BIT 3
00	0	BkRst_C00_s	BkRst_C0P0_s	BkRst_C0P1_s	BkRst_C0P2_s	BkRst_C0P3_s
00	1	BkRst_C01_s	BkRst_C0P4_s	BkRst_C0P5_s	BkRst_C0P6_s	BkRst_C0P7_s
01	0	BkRst_C10_s	BkRst_C1P0_s	BkRst_C1P1_s	BkRst_C1P2_s	BkRst_C1P3_s
01	1	BkRst_C11_s	BkRst_C1P4_s	BkRst_C1P5_s	BkRst_C1P6_s	BkRst_C1P7_s
1X	NA	NA	NA	NA	NA	NA

FIG. 9

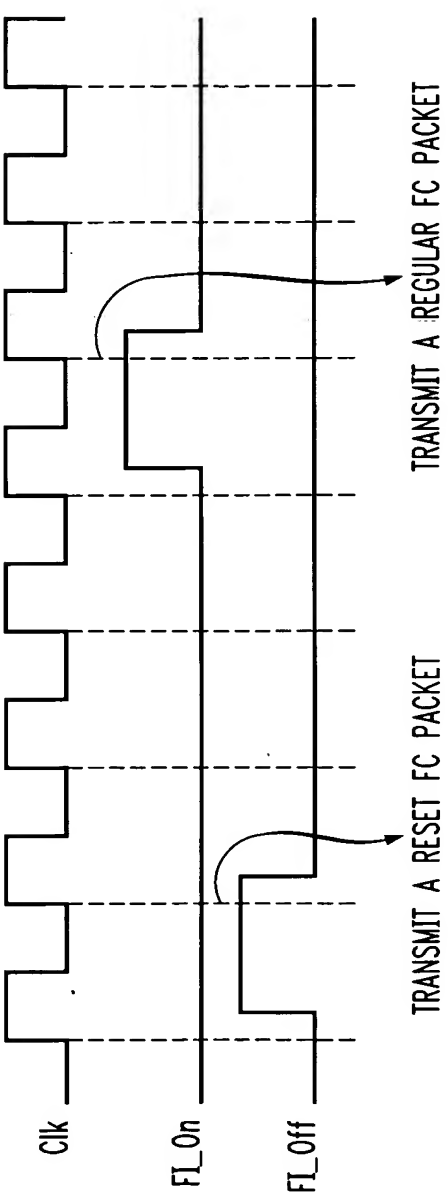


FIG. 10

ADDR DECODER FOR A-N REGISTER INFORMATION

CHANNEL ADDR[1:0]	NIBBLE ADDR/CTRL	[3:0]	BIT 0	BIT 1	BIT 2	BIT 3
00, 01, 10, 11	0, 1	AN_D0_s	TxLreg_s[0]	TxLreg_s[1]	TxLreg_s[2]	TxLreg_s[3]
	XData_s	AN_D1_s	TxLreg_s[4]	TxLreg_s[5]	TxLreg_s[6]	TxLreg_s[7]
	Xconfig_s	AN_D2_s	TxLreg_s[8]	TxLreg_s[9]	TxLreg_s[10]	TxLreg_s[11]
	0	AN_D3_s	TxLreg_s[12]	TxLreg_s[13]	TxLreg_s[14]	TxLreg_s[15]

FIG. 11

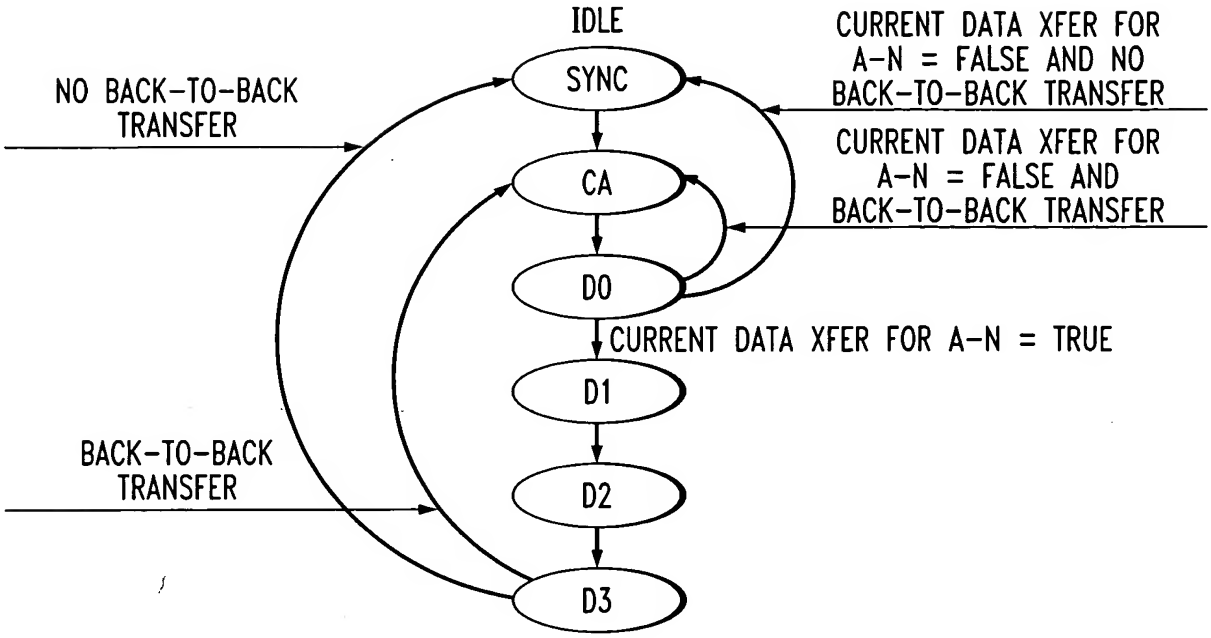


FIG. 12

CONTROL INFORMATION DECODE

Ctrl[2:0]	CONTROL TYPE
3'b000	SYNC
3'b001	CRS
3'b010	AN_D
3'b011	FcTxOFF
3'b100	FI_On
3'b101	FI_Off
3'b110	BkRst
3'b111	RESERVED

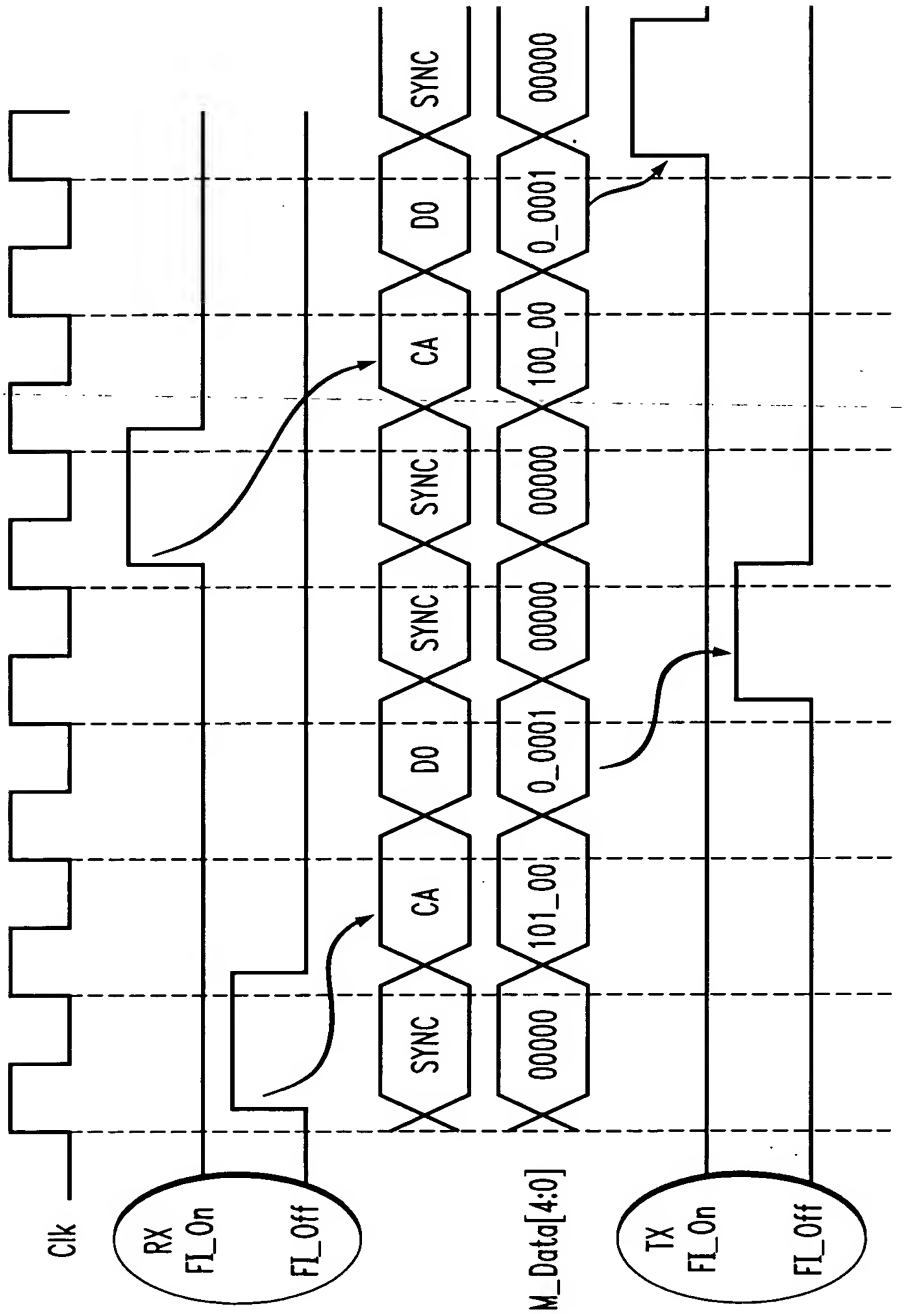


FIG. 13

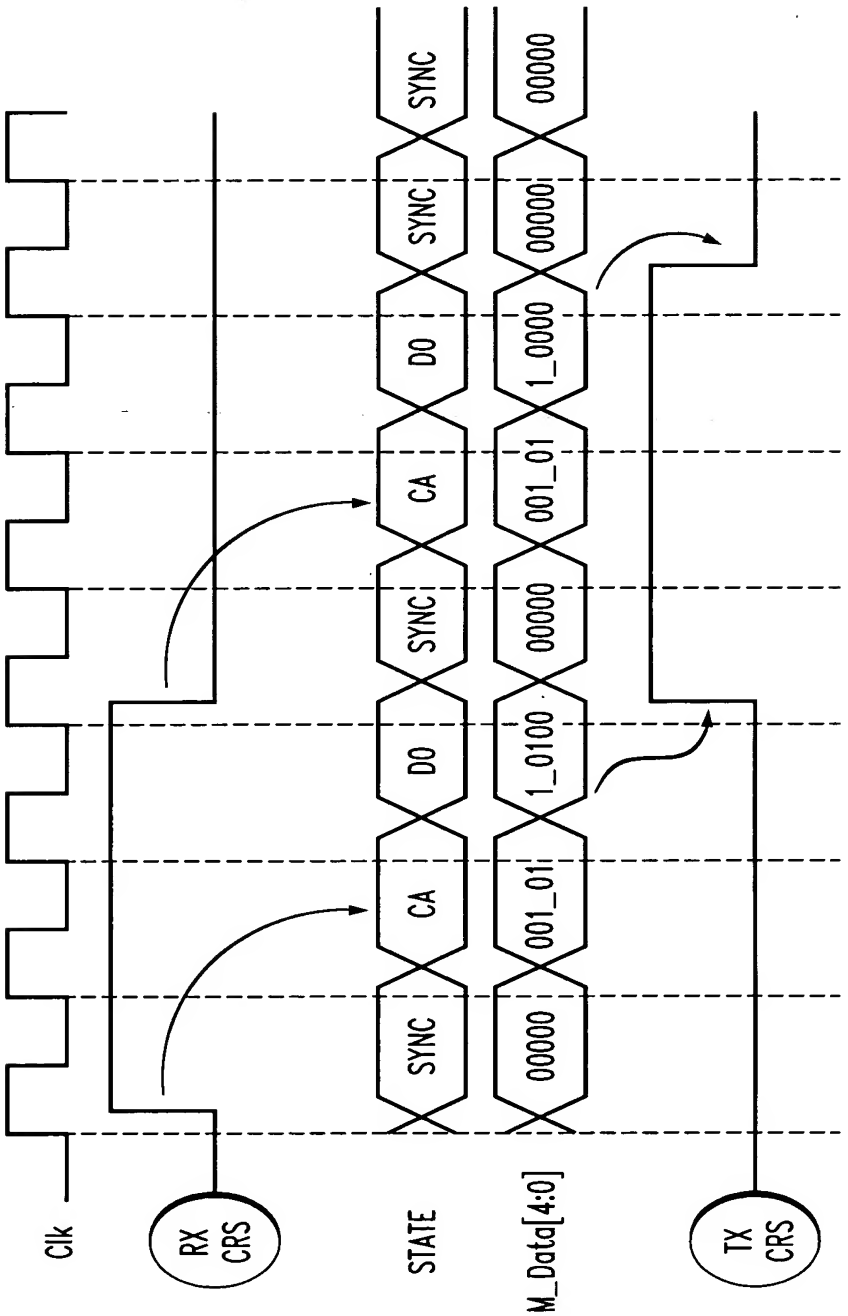


FIG. 14

FIG. 15

EXAMPLE WAVEFORM FOR T/R INTERFACE

CLOCK	x+1	x+2	x+3	x+4	x+5
M_DATA[4:0]	5'b001_00	5'b0_1010	5'b101_10	5'b0_0001	5'b000_00
PHASE	CA	DATA	CA	DATA	SYNC
DECODED CTRL	CRS	NA	FI_Off	NA	NA
CHANNEL ADDR	CHANNEL 0	NA	CHANNEL 2	NA	NA
NIBBLE A/C	NA	0	NA	NA	NA
DATA[3:0]	NA	4'b1010	NA	4'b0001	NA
		CRS_C00_s		FO_C20_s	

FIG. 16

EXAMPLE FOR A-N INFO ON T/R INTERFACE FOR CHANNEL 3, NIB ADDRESS 0

CLOCK	x+1	x+2	x+3	x+4	x+5	x+6
M_DATA[4:0]	5'b010_11	5'b0_1010	5'b1_0010	5'b0_1110	5'b0_1101	5'b000_00
PHASE	CA	DATA	DATA	DATA	DATA	SYNC
DECODED CTRL	A-N	NA	NA	NA	NA	NA
CHANNEL ADDR	CHANNEL 3	NA	NA	NA	NA	NA
NIBBLE A/C	NA	0	XData_s	XConfig_s	0	NA
DATA[3:0]	NA	4'b1010	4'b0010	4'b1110	4'b1101	NA
		AN_D0_s	AN_D1_s	AN_D2_s	AN_D3_s	